In the Claims:

Cancel claims 15-27 and 36-59 without prejudice.

Add new claims 60-107 as follows.

60. (New) A circuit, comprising:

an input terminal coupled to receive a first and a second group of signals, each group having a respective sequence;

a first output terminal coupled to receive the first group of signals during a first time; and

a second output terminal coupled to receive a third group of signals having a sequence during the first time, the third group of signals comprising a transform of the second group of signals.

61. (New) A circuit as in claim 60, wherein each signal of each group of signals comprises a symbol.

62. (New) A circuit as in claim 61, wherein each symbol is a quadrature phase shift keyed symbol.

63. (New) A circuit as in claim 60, wherein the transform of the second group comprises conjugation and reversal of order in time.

64. (New) A circuit as in claim 60, wherein the transform of the second group comprises conjugation, negation, and reversal of order in time.

65. (New) A circuit as in claim 60, wherein the first output terminal is coupled to receive the second group of signals during a second time, and wherein the second output

terminal is coupled to receive a fourth group of signals having a sequence during the second time, the fourth group of signals comprising a transform of the first group of signals.

66. (New) A circuit as in claim 65, wherein the transform of the first group comprises conjugation and reversal of order in time.

67. (New) A circuit as in claim 65, wherein the transform of the first group comprises conjugation, negation, and reversal of order in time.

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68. (New) A circuit as in claim 60, comprising a symbol mapper circuit having an input terminal coupled to receive a first sequence of data bits, the symbol mapper circuit producing the first and second groups of signals.

69. (New) A circuit as in claim 68, wherein each signal corresponds to two of the data bits.

70. (New) A circuit as in claim 68, comprising an interleaver circuit having an input terminal coupled to receive a second sequence of data bits, the interleaver circuit producing the first sequence comprising data bits of the second sequence having a different order.

71. (New) A circuit as in claim 70, comprising a channel encoder circuit having an input terminal coupled to receive a third sequence of data bits, the channel encoder circuit encoding the third sequence to produce the second sequence of data bits.

72. (New) A circuit as in claim 70, wherein the channel encoder circuit encodes the third sequence of data bits with a convolutional code.

73. (New) A circuit as in claim 70, wherein the channel encoder circuit encodes the third sequence of data bits with a block code.

74. (New) A circuit as in claim 70, wherein the channel encoder circuit encodes the third sequence of data bits with a turbo code.

75. (New) A circuit as in claim 60, wherein the first and second group of signals are encoded by one of a pseudo noise code, a Walsh code, and a combination of a pseudo noise code and a Walsh code.

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76. (New) A circuit as in claim 75, wherein the code applied to the second group of signals is reversed in time from the code applied to the first group of signals.

77. (New) A circuit as in claim 75, wherein the first and second output terminals are arranged for connection to respective first and second antennas.

78. (New) A method of processing signals, comprising the steps of:

applying a respective plurality of signals to each of a plurality of encoder circuits;

producing a first group of the respective plurality of signals at a first output terminal of said each of a plurality of encoder circuits;

producing a transformed second group of the respective plurality of signals at a second output terminal of said each of a plurality of encoder circuits; and

modulating the first group and the transformed second group each of the respective plurality of signals by a respective code corresponding to said each of a plurality of encoder circuits.

79. (New) A method as in claim 78, wherein each signal of the respective plurality of signals comprises a symbol.

80. (New) A method as in claim 79, wherein each symbol is a quadrature phase shift keyed symbol.

81. (New) A method as in claim 78, wherein the transformed second group comprises conjugation and reversal of order in time of a second group of the respective plurality of symbols.

82. (New) A method as in claim 78, wherein the transformed second group comprises conjugation, negation, and reversal of order in time of a second group of the respective plurality of symbols.

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83. (New) A method as in claim 78, comprising the steps of:

producing a second group of the respective plurality of signals at the first output terminal of said each of a plurality of encoder circuits;

producing a transformed first group of the respective plurality of signals at the second output terminal of said each of a plurality of encoder circuits; and

modulating the second group and the transformed first group each of the respective plurality of signals by the respective code corresponding to said each of a plurality of encoder circuits.

84. (New) A method as in claim 83, wherein the transformed second group comprises conjugation and reversal of order in time of a second group of the respective plurality of symbols, and wherein the transformed first group comprises conjugation, negation, and reversal of order in time of the first group of the respective plurality of symbols.

85. (New) A method as in claim 78, comprising the steps of:

adding each said first group of the respective plurality of signals at each said first output terminal, thereby producing a first output signal; and

adding each said transformed second group of the respective plurality of signals at each said second output terminal, thereby producing a second output signal.

86. (New) A method as in claim 85, comprising the step of encoding the first and second output signals with one of a pseudo noise code, a Walsh code, and a combination of a pseudo noise code and a Walsh code.

87. (New) A method as in claim 86, wherein the code applied to the second output signal is reversed in time from the code applied to the first output signal.

88. (New) A method as in claim 86, comprising the steps of:

applying the first output signal to a first antenna; and

applying the second output signal to a second antenna.

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89. (New) A circuit, comprising:

an input terminal coupled to receive a first and a third group of signals during a first time and coupled to receive a second and a fourth group of signals during a second time, the third group comprising a transform of the second group, the fourth group comprising a transform of the first group, each group having a respective sequence;

a first output terminal coupled to receive the first group of signals; and

a second output terminal coupled to receive the second group of signals.

90. (New) A circuit as in claim 89, wherein each signal of each group of signals comprises a symbol.

91. (New) A circuit as in claim 90, wherein each symbol is a quadrature phase shift keyed symbol.

92. (New) A circuit as in claim 89, wherein the transform of the second group comprises conjugation and reversal of order in time.

93. (New) A circuit as in claim 89, wherein the transform of the fourth group comprises conjugation, negation, and reversal of order in time.

94. (New) A circuit as in claim 89, comprising:

a first block equalizer circuit having an input terminal coupled to the first output terminal and having an output terminal; and

a second block equalizer circuit having an input terminal coupled to the second output terminal and having an output terminal.

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95. (New) A circuit as in claim 94, wherein the first and second block equalizer circuits multiply the respective first and second groups of signals by a common matrix.

96. (New) A circuit as in claim 94, comprising:

a first block despreader circuit having an input terminal coupled to the output terminal of the first block equalizer circuit; and

a second block despreader circuit having an input terminal coupled to the output terminal of the second block equalizer circuit.

97. (New) A circuit as in claim 96, wherein the first and second block despreader circuits are coupled to receive a common code.

98. (New) A circuit as in claim 96, wherein the first block despreader circuit is coupled to receive a first code having a sequence and the second block despreader circuit is coupled to receive the first code having the sequence reversed in time.

99. (New) A circuit as in claim 89, comprising:

a first block despreader circuit having an input terminal coupled to the first output terminal and having an output terminal; and

a second block despreader circuit having an input terminal coupled to the second output terminal and having an output terminal.

100. (New) A circuit as in claim 99, wherein the first and second block despreader circuits are coupled to receive a common code.

101. (New) A circuit as in claim 99, wherein the first block despreader circuit is coupled to receive a first code having a sequence and the second block despreader circuit is coupled to receive the first code having the sequence reversed in time.

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102. (New) A circuit as in claim 99, comprising:

a first block equalizer circuit having an input terminal coupled to the output terminal of the first block despreader circuit; and

a second block equalizer circuit having an input terminal coupled to the output terminal of the second block despreader circuit.

103. (New) A circuit as in claim 102, wherein the first and second block equalizer circuits multiply the respective first and second groups of signals by a common matrix.

104. (New) A circuit as in claim 89, comprising a despreader circuit coupled to receive the first, second, third, and fourth groups of signals, the despreader circuit producing the first and the third group of signals during the first time and producing the second and the fourth group of signals during the second time.

105. (New) A circuit as in claim 104, wherein the despreader circuit is arranged to receive the first, second, third, and fourth groups of signals from a remote transmitter.

106. (New) A circuit as in claim 89, comprising a rake circuit, the rake circuit including a memory circuit arranged to store the first, second, third, and fourth groups of signals.

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107. (New) A circuit as in claim 106, wherein the rake circuit is arranged to combine like signals of the respective first, second, third, and fourth groups of signals received from a remote transmitter along multiple paths.